Keysight Technologies
PCI Express® Design and Test from Electrical to Protocol


Thoroughly Simulate, Characterize and Validate PCI Express Designs

KEYSIGHT TECHNOLOGIES
Unlocking Measurement Insights

HARDWARE + SOFTWARE + PEOPLE = PCIe® INSIGHTS

Realize Your Best Design

In digital standards, every generation change puts new risks in your path. We see it firsthand when creating our products and working with engineers like you. The Keysight Technologies, Inc. solution set for high-speed digital test is a combination of software, instrumentation and broad expertise built on our early and ongoing involvement with industry experts.

PCI Express® technology has been implemented broadly in systems requiring high-speed data transfer, such as video or graphics. Initially embraced by high-performance desktop and server systems, it is now finding a home in embedded applications. Specifications and compliance tests are defined by the PCI Special Interest Group (PCI-SIG®) (see Figure 1).

The overwhelming concern for designers is interoperability and backward compatibility. You need tools to validate the parametric and protocol aspects of your designs to make sure your design is in compliance, and to see how close the design performance is to specification.

Higher data rates increase signal integrity symptoms like reflections and crosstalk, causing signal degradation and timing issues. A shorter clock cycle means a smaller jitter budget, so reducing jitter is far more complex. Likewise, as PCI Express is used in more diverse environments, the protocol layer capabilities are increasing.

When you can gain insight to your design early in the design cycle, you can take corrective action quickly to make sure you meet product quality, interoperability and time-to-market goals. By sharing our latest experiences, we can help enhance your ability to create products you'll be proud of. Work with Keysight and realize your best design.

PCI Express version	1.0a	1.1	2.0	3.0	4.0
Data transfer rate	2.5 GT/s	2.5 GT/s	2.5 and 5.0 GT/s	2.5, 5.0 and 8.0 GT/s	2.5, 5.0, 8.0 and 16.0 GT/s
Data fundamental frequency	1.25 GHz	1.25 GHz	2.5 GHz	4.0 GHz	8.0 GHz
Data encoding	PRBS16 scrambling and 8b/10b coding	PRBS16 scrambling and 8b/10b coding	PRBS16 scrambling and 8b/10b coding	2.5 GT/s and 5 GT/s: PRBS16 scrambling and 8b/10b coding 8 GT/s: PRBS23 Scrambling and 128b/130b coding	2.5 GT/s and 5 GT/s: PRBS16 scrambling and 8b/10b coding 8 and 16 GT/s: PRBS23 Scrambling and 128b/130b coding
Total bandwidth for x16 link	~6.4 GB/s	~6.4 GB/s	~12.8 GB/s	~25.6 GB/s	~32 GB/s
Key changes	Initial release	Tighter jitter and reference clock tests	Speed, Cable specification, PLL bandwidth test, tighter jitter and reference clock tests, new de-emphasis levels	Speed, higher PLL bandwidth, more complex de-emphasis, PRBS23 scrambling	Speed, shorter channel, single connector, more transmit de-emphasis states, more taps on DFE, much smaller Rx eye height

Figure 1. PCI Express technologies and key specifications

Key Task

PCI Express design can be segmented into physical layer, data link layer and transaction layer. For Card Electromechanical (CEM) specifications, the PCI-SIG provides the Compliance Base Board (CBB), the Compliance Load Board (CLB), and the SigTest software to facilitate electrical compliance testing.

Protocol compliance requires a different approach. While the PCI-SIG workshops provide a formal verification of your design, you need to perform compliance tests before attending a workshop.

Keysight offers solutions to meet your needs in the electrical physical layer, protocol layer, and functional test (see Figure 2).

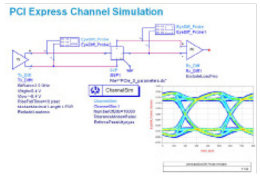
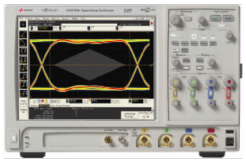
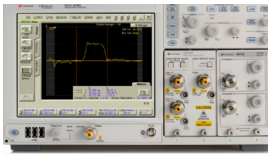
Physical layer: interconnect design	Physical layer: transmitter test	Physical layer: receiver test	Data link/transaction layer
			
– ADS Design Software with W2352 PCIe compliance test bench	– Infiniium V-Series Oscilloscopes – N5393D PCI Express electrical compliance software – EZJIT plus and High-speed serial data analysis software – 86100D DCA-X with 86100DU-400 PLL measurement software	– J-BERT M8020A high-performance BERT – J-BERT N4903B high-performance serial BERT with N4916B de-emphasis signal converter – N5990A Automated compliance and device characterization test software	– U4301B PCIe analyzer – U4305A/B PCIe exerciser & PCIe LTSSM exerciser – N5306A protocol analyzer for PCIe 1.0 and 2.0 – PCIe analyzer – PCIe exerciser – PCIe jammer – Protocol compliance test card (PTC)
			
– 86100D DCA-X/TDR – E5071C-TDR ENA network analyzer			

Figure 2. Keysight PCI Express design and test solutions

Applying expertise

Keysight has decades of experience in digital, RF and protocol engineering. We understand the reflections, insertion and return loss, jitter budget, timing margins and other issues that designers have to face in high data rate standards. Our protocol expertise is leveraged from our long time support of the PCI standards. As an active member of the PCI-SIG, with consistent participation in workshops and specification issues, Keysight has a solid understanding of the physical layer, data link layer and transaction layer used by PCI Express.

Keysight has a long history of collaborative innovation with industry leaders. It puts Keysight in a position to develop tools that meet the physical challenges, are customized to the needs of the standard, and are relevant to the way designers and developers need to use them.

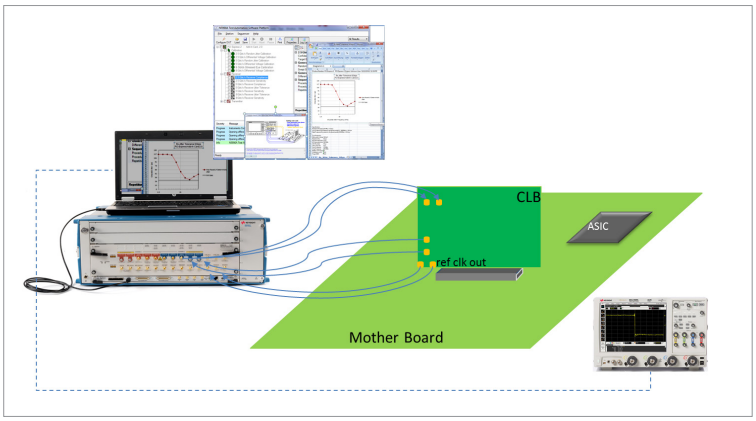


Figure 3. J-BERT M8020A streamlines complex receiver test setups. The example shows a PCIe 3 (8 GT/s) mother board RX test (CEM spec) with J-BERT M8020A connected via a compliance load board (CLB). J-BERT M8020A provides built-in de-emphasis, jitter sources, common-mode and differential mode interference (CMI, DMI), reference clock multiplier, clock recovery and continuous time linear equalizer (CTLE) – everything that is needed is built-in and calibrated.

Complete, reliable test coverage

What makes Keysight solutions so compelling is that they were developed to match the application's specific needs – oscilloscopes to verify signal integrity and jitter, BERTs and pattern generators to create complex stimulus signals and to test receivers (see Figure 3), protocol exercisers/analyzers to debug packets, time-domain reflectometer (TDR) and a vector network analyzer (VNA) to characterize impedance, and EDA software integrated with compliance applications to enable the same tests on simulated designs and manufactured hardware.

The quality of Keysight solutions is the key to easier, faster and more confident testing of your PCI Express designs. Accurate results reduce the number of design cycles to help you get to market faster, and they ensure robust designs that uphold your competitive advantage in the market.

Physical Layer: Transmitter Test

Validating PCI Express performance involves characterizing the reference clock and data signals. Your product must successfully pass “Gold Suite” testing – a superset of what the PCI-SIG SigTest tests – at a PCI-SIG workshop using the official PCI-SIG approved test fixtures. Key parameters are rise-time, amplitude, eye width, jitter and Phase-Locked Loop (PLL) bandwidth and peaking.

Measure quickly, with confidence

Whether you are troubleshooting, capturing contiguous waveforms, ensuring correct operation, or proving compliance, an oscilloscope with low noise, low jitter, and high probe accuracy is critical for measurement accuracy. Eye diagram tests examine the minimum eye opening for adequate operation. Reference clock jitter analysis helps ensure that the system bit error ratio (BER) can be achieved.

Keysight’s Infiniium V-Series oscilloscopes provide the lowest noise floor, jitter noise floor, and trigger jitter by a real-time oscilloscope in the industry. The industry’s longest 160-bit sequence provides an effective event trigger to find and debug the most challenging problems in your design (see Figure 4). The N5400A EZJIT Plus jitter software includes the SigTest clock recovery algorithm for accurate results. Add the Keysight N5393D PCI Express electrical performance compliance and validation software to simplify setup, perform compliance tests, and produce an HTML report, complete with screenshots, to easily share your results (see Figure 5).

Precise PLL bandwidth analysis

To ensure interoperability, it is necessary to control the PLL bandwidth of your design. Accurate characterization of PLL bandwidth and peaking requires a receiver, such as an oscilloscope, that can accurately measure injected sinusoidal jitter. An alternative approach is to use a spectrum analyzer and signal generator to sweep the PLL response.

The Keysight 86100D Infiniium DCA-X wideband oscilloscope mainframe with the 86108B precision waveform analyzer module offer the industry’s lowest intrinsic jitter of < 50 fs. The 86108B hardware clock recovery circuit features a differential phase detector to demodulate the incoming jitter, which is post-processed by the 86100DU-400 PLL and jitter spectrum measurement software to measure phase noise and jitter transfer function directly (see Figure 6). This approach is used in the PCI-SIG Gold Suite to fully characterize device PLLs for conformance to specification.

The Keysight Infiniium V-Series oscilloscopes provide best-in-class signal integrity, most advanced probing system, longest hardware serial trigger and broadest software and application solutions in the industry.

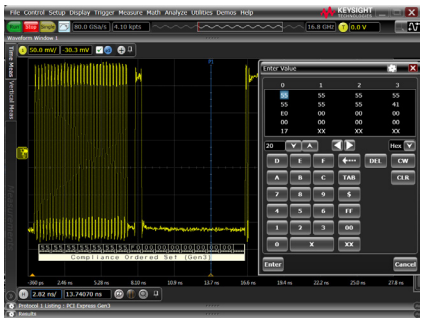


Figure 4. **V-Series’ hardware serial trigger finds a PCI Express Gen 3 compliance ordered set symbol that is 130-bit long (PCIe Gen 3 uses 128b/130b encoding).**

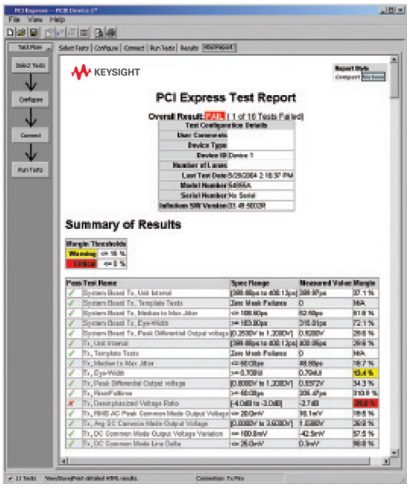


Figure 5. N5393D PCI Express electrical test software generates a summary report for your device quickly, including waveforms and the margin of the result to provide further insight

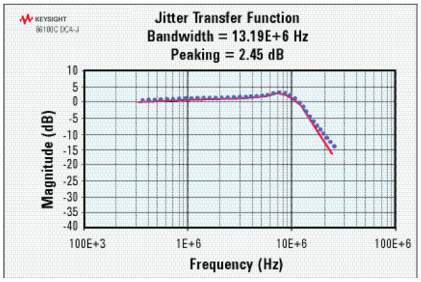


Figure 6. PLL bandwidth test with the 86100D DCA-X and 86108B precision waveform analyzer

Physical Layer: Receiver Test

The receiver in a digital transmission system must extract the digital content from its input signal with a very low bit error ratio. It typically sees a heavily degraded signal due to the channel's high-frequency loss characteristics. A robust receiver must tolerate these distorted signals and make the correct bit decisions. PCI Express uses a jitter tolerance test, based on stressed eye measurements, to qualify receiver performance.

Quick, accurate jitter tolerance test

To fully characterize a receiver's jitter tolerance, you need a pattern generator to create signals to bring the device into loop-back mode, generate a reference clock with spread-spectrum capability, and create calibrated, compliant jitter injection and de-emphasis to emulate receiver stress conditions. Measurement accuracy will be determined by your ability to control these signal attributes. The more precise the source, the better the understanding of your receiver design.

The Keysight J-BERT M8020A and the J-BERT N4903B offer fully integrated and calibrated precision jitter sources. They provide quick, authentic, worst-case jitter and amplitude signals, including random, sinusoidal, and periodic jitter, plus Inter-Symbol Interference (ISI) to emulate motherboard conditions. The built-in jitter tolerance test routines let you quickly test your receiver (see Figure 7). You can emulate a transmitter with de-emphasized PCI Express signals to further characterize your receiver (see Figure 8). For J-BERT M8020A, the de-emphasis capability is integrated in order to simplify the test setup. The N4916B de-emphasis converter is required when using J-BERT N4903B.

Simplifying complex tasks

With PCI Express, its versatility shows when you create multi-lane designs. Additional lanes increase throughput, but complicate receiver design and debug. Are you able to emulate multi-lane signals? Do you have to test each lane separately, or is there a way to automate the process?

The Keysight M8020A J-BERT is a modular BERT platform that can be configured with multiple data generators and data analyzers for multi-lane testing.

You can automate the receiver test, or create a complete transmitter/receiver compliance test, with the N5990A test automation software (see Figure 9). It controls the J-BERT M8020A, J-BERT N4903B, Infiniium oscilloscopes and other Keysight solutions.

The Keysight J-BERT M8020A and J-BERT M4903B have fully integrated and calibrated precision jitter sources for automated jitter tolerance testing.

PCI Express receiver test setups based on J-BERT M8020A

Most receiver test solutions so far, including the J-BERT N4903B-based setup, require additional instruments to complete the stressor set offered by the BERT.

The J-BERT M8020A offers built-in CM-SI and DM-SI and eliminates the need for additional non ISI stressors. J-BERT M8020A has an integrated PCI Express compliant reference clock multiplier which can generate the necessary clock for the BERT from the system's 100 MHz reference clock. The multiplier's PLL is high enough to transfer SSC, allowing testing of systems with SSC turned on.

The extension of stress sources, integration of de-emphasis into each pattern generator data output, as well as equalizing capabilities into each error detector data input, and integrated reference clock multipliers simplify the PCI Express receiver test setups greatly, compared to its predecessor, J-BERT N4903B. The M8041A BERT module of the J-BERT M8020A BERT system offers data ranges up to 8.5 Gb/s or up to 16.2 Gb/s. The 16.2 Gb/s version allows testing of receivers for all four transfer rates. The J-BERT M8020A helps in mastering PCI Express receiver designs.

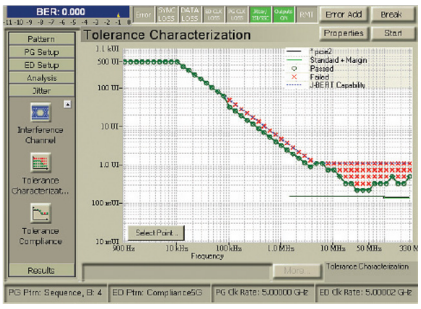


Figure 7. A jitter tolerance measurement using the J-BERT N4903B with sinusoidal jitter from 1 kHz to 300 MHz

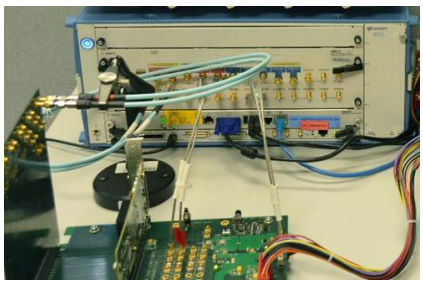


Figure 8. Jitter tolerance test setup using the J-BERT M8020A.

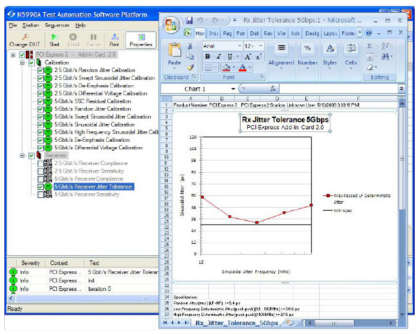


Figure 9. Automated PCI Express receiver test using the N5990A test automation software

Physical Layer: Interconnect Design

As data rates increase, you need to pay special attention to your board design to minimize signal integrity problems. Long trace lengths cause signal attenuation, rise-time degradation, and jitter. Impedance transitions between a trace and via can cause reflections and crosstalk. You need to use tools that are more commonly used by high-frequency engineers – a time-domain reflectometer (TDR), a vector network analyzer (VNA), and high-frequency simulation software.

Accurate impedance measurements

Crosstalk, attenuation, impedance and frequency response are commonly measured using either a TDR or a VNA. To ensure optimum accuracy, these instruments employ a calibration sequence to remove the effects of any cables or fixtures that connect the TDR or VNA to the device under test.

The Keysight 86100D DCA-X with the 54754A differential TDR/TDT module provides a quick, intuitive view of impedance discontinuities. By switching to frequency mode, you can examine the calibrated S-parameters for transmission and impedance performance of channels, cables, and connectors (see Figure 10). To improve accuracy, the 86100C TDR utilizes a unique calibration process that removes the effects of cabling, allowing you to isolate your device from the test system.

The Keysight E5071C ENA network analyzer with the enhanced time domain analysis option provides a one-box solution for interconnect analysis. Both time domain impedance and frequency domain S-parameters can be measured and eye-diagram analysis can be performed as well. The VNA offers higher accuracy than a TDR due to its higher dynamic range and more complete calibration approach, which is important when measuring low insertion loss or low reflection devices.

In addition, the simple and intuitive user interface designed for digital engineers, as well as the high ESD robustness of the VNA, provides a unique solution for your tough measurement challenges.

Predict interconnect performance through simulation

High-frequency engineers commonly use RF simulation tools to predict the effects of transitions, connectors, and traces. Digital designers instead rely upon SPICE-based simulators to account for analog effects. These simulators can sometimes include high-frequency S-parameter data, but rarely match an RF simulator in accurately predicting the high-frequency impact of every element in their circuit.

The Keysight Advanced Design System (ADS) has several features optimized for the high-speed digital designer. An add-on for ADS (W2352 PCI Express compliance test bench) provides a quick vehicle to start a PCI Express design. You can analyze complete serial links by co-simulating individual components, each at its most appropriate level of abstraction: link, circuit or physical level (see Figure 11). Import measured S-parameters as circuit elements for more accuracy. Make analyses quickly by connecting to the Infiniium compliance applications from Keysight oscilloscopes to ensure you are using the very same compliance tests on your software simulated design as on the subsequently manufactured hardware.

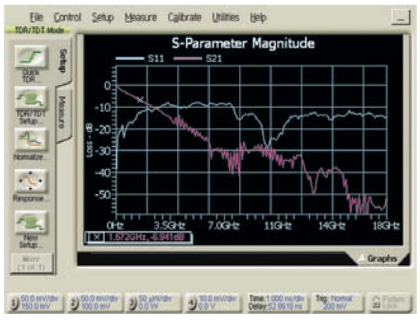


Figure 10. S-parameters can be automatically generated from the 86100D DCA-X TDR measurement software

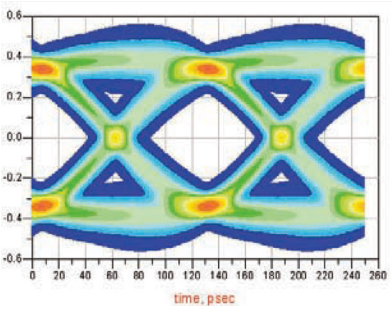


Figure 11. ADS simulates a PCI Express 3.0 channel, with the resultant differential eye measurement

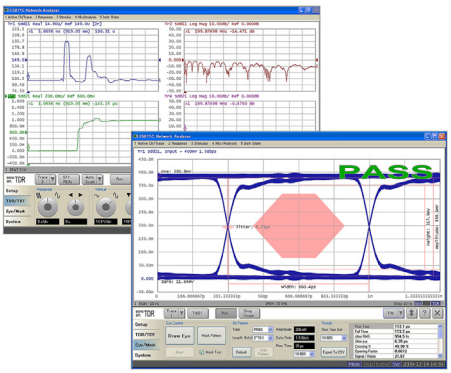


Figure 12. ENA Option TDR provides time domain, frequency domain, and eye diagram analysis capability.

Data Link/Transaction Layer: Protocol Validation and Stress Test

Protocol validation occurs at the physical layer, data link layer and transaction layer, each having its own challenges. Validation requires generating the appropriate stimulus – emulating a root-complex when testing an add-in card, or an end device for testing a root-complex device. The PCI-SIG stipulates the use of a Protocol Test Card (PTC) for the mandatory tests, but you will likely want to characterize your design more extensively to ensure interoperability.

Validate protocol quickly and easily

In addition to the mandatory protocol compliance tests, the PCI-SIG recommends over a hundred more to properly characterize your design. A key area of test is Link Training and Status State Machine (LTSSM). It is responsible for establishing the link between two components; ensuring that the link is established, and that the parameters are negotiated and agreed between the two components. With many states and sub-states, it is important to ensure that each of the state transitions is tested.

The Keysight LTSSM exerciser can help you quickly validate complex and hard to test transitions of the LTSSM in your design, including dynamic link width changes (see Figure 12). The same hardware can also be used as the exerciser for PCIe. Keysight's PCIe exerciser can emulate either root-complex or endpoint to allow testing of any type of DUT for PCIe 3.0, PCIe 2.0 and PCIe 1.0. With controllable packet generation and error insertion, the exerciser is crucial to fully validating the design of your device (see figure 13).

How robust is your design?

Your system seems to be working, but you can't reproduce an intermittent failure. You need it to be more robust and recover from all errors correctly. This is challenging given the need to reduce validation time and the difficulty of emulating a real-life setup. Ideally you want to inject errors into real-life traffic, see how your design responds, and improve the software accordingly.

The Keysight U4305A PCI Express Exerciser can be used to replace a device on the link. Insert it into a working system, and start testing. Detailed reporting helps clearly define the source of problem for faster debug. Integrate with the U4301B protocol analyzer for deep root cause analysis.

PTC (Protocol Test Card) operation PCIe link and transaction tests as defined by the PCI-SIG provide easy-to-understand pass/fail results.

NVMe Emulation

Validation of NVMe devices or systems is simplified with the use of the NVMe tools available on the U4305A PCIe exerciser. Verify how the NVMe controller handles admin requests such as queue management or controller initialization. Keysight is proud to implement the NVMe conformance tests as defined by the University of New Hampshire (UNH) Interoperability Lab (IOL). These tests provide pass/fail/warning results with detailed diagnostic information to improve NVMe validation (see Figure 14).

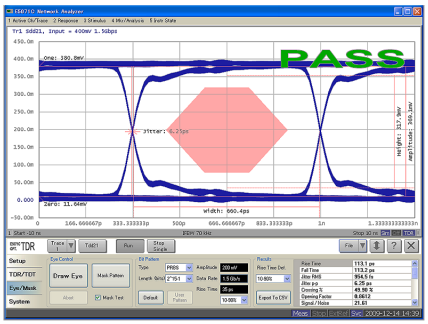


Figure 13. Configuring LTSSM tests is quick and easy with the LTSSM exerciser for PCIe 3.0 and PCIe 2.0

Figure 14. Thoroughly validate the device under test (DUT) with Keysight's exerciser.

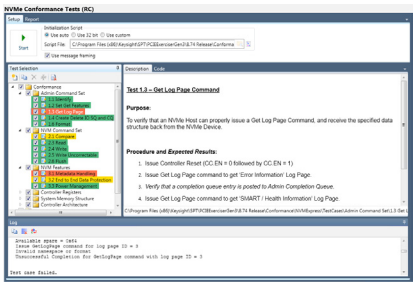


Figure 15. The NVMe conformance test suite 1.1 testing is implemented in an easy-to-use validation framework.

Data Link/Transaction Layer: Protocol Debug

When protocol errors are detected, you need to analyze why, then correct them. To do this, you need to access the signals, trigger on specific events, capture the traffic reliably, and view the results for quick interpretation. At speed, in-system test requires high-performance probing solutions combined with a versatile protocol analyzer.

Quickly find and solve protocol issues

Debugging PCI Express protocol means capturing traffic at speed and during power management transitions. A protocol analyzer will need to lock onto traffic quickly, then trigger on a unique protocol sequence. Debugging lower level problems such as power management, requires exceptionally fast lock times. Once you capture the traffic, you'll want to view the data at different levels of abstraction to assess what is happening.

The Keysight PCI Express protocol analyzer is a powerful tool for debug. The analyzer works with x1 to x16 designs, with advanced triggering capabilities to reduce the time needed to detect difficult-to-find errors (see Figure 15). Use the lane or packet views to observe data to find issues associated with entering and exiting out of low-power states (see Figure 16). For higher layer problems, such as data integrity, the transaction viewer lets you observe all the data from multiple completions together in one location for easy analysis.

Accessing signals for real-time debug

A key challenge in PCI Express protocol debug is gaining access to the signals in a non-invasive manner. Where you probe, and how you probe, are dependent upon your system design. Mid-bus probes provide access to traffic, but should not impact signal quality. Slot interposers need to pass signals passively over a long trace and not change the signals.

Keysight's PCI Express protocol analyzer provides a wide range of probing solutions. Keysight's U4301B PCIe Gen3 analyzer probing solutions include SFF-8639, M.2, and slot interposers, as well as mid-bus and flying lead probes.

Keysight's Gen3 probes utilize Keysight's unique ESP (Equalization Snoop Probe) technology, with the ability to tune the equalization algorithm used according to the type of channel the analyzer is monitoring. This ensures that the data captured in the analyzer is exactly what is on the wire. Without this capability, at 8GT/s, there is a high likelihood of misrepresentation of the data on the bus, which can lead to wasted hours, if not days in the validation cycle. Both mid-bus probes and slot interposer probes are available for Gen3 measurements.

The Keysight U4301B PCIe analyzer is the industry's most complete tool for LTSSM, flow control, and performance analysis of your PCIe devices.

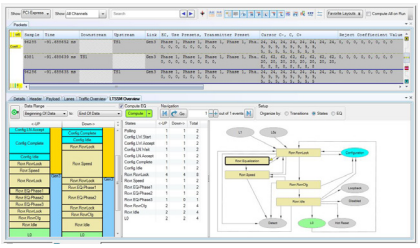


Figure 16. LTSSM analysis is made easy with detailed tracking of each state transition displayed in a linear state-view, state transition table, and state bubble chart.

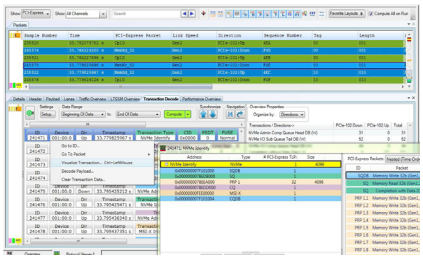


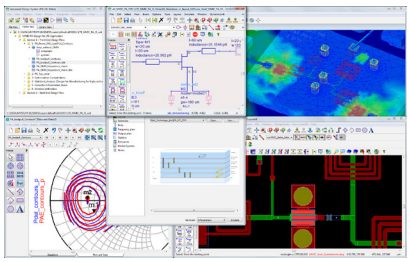
Figure 17. NVMe transaction information provides easy-to-understand displays of NVMe payloads and PRP messages. An overview of all transactions enables instant access to all messages in the capture trace .

Figure 18. The N4240 Series mid-bus probes feature Soft Touch technology for non-invasive probing

Keysight PCI Express Solutions

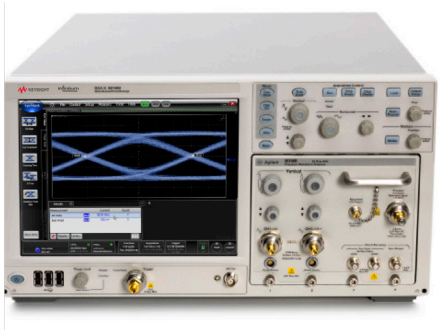
Advanced Design System (ADS)

With a complete set of simulation technologies ranging from frequency-, time-, numeric and physical domain simulation to electromagnetic field simulation, ADS lets designers fully characterize and optimize designs. The single, integrated design environment provides system, circuit, and electromagnetic simulators, along with schematic capture, layout, and verification capability -- eliminating the stops and starts associated with changing design tools in mid-cycle.



86100D Infiniium DCA-X wide-bandwidth oscilloscope with TDR and PLL analysis

The Keysight 86100D DCA-X combines precision waveform analysis, jitter measurements, and TDR and S-parameter measurements with one-button ease-of-use. The Keysight 86108B precision waveform analyzer provides ultra-low jitter measurements with integrated hardware clock recovery for accurate PLL analysis. The Keysight 54754A differential TDR/TDT module provides real-time impedance and crosstalk measurements.



E5071C ENA Network Analyzer Option TDR

The Keysight ENA Option TDR provides a one-box solution for high-speed serial interconnect analysis: Time domain, frequency domain, and eye diagram analysis. For signal integrity design and verification, it brings three breakthroughs; simple and intuitive operation, fast and accurate measurements, and high ESD robustness.

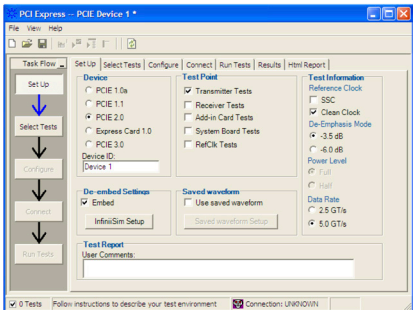
Infiniium V-Series Oscilloscopes

Infiniium V-Series oscilloscopes incorporate innovative technology designed to deliver superior measurements. The new 12.5 Gb/s, longest 160-bit hardware serial trigger and world's fastest 20 GSa/s digital channels will provide timely validation and debug. This oscilloscope's low-noise front end technology, advanced InfiniiMax III/III+ Series probes and revolutionary voltage termination adapter provide up to 33 GHz performance with the industry's best signal integrity.

Keysight PCI Express Solutions (continued)

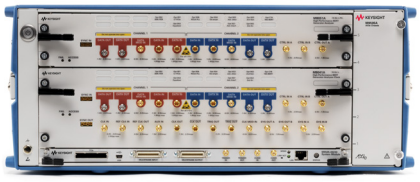
N5393D PCI Express electrical compliance test software

The Keysight N5393D PCI Express electrical performance validation and compliance software for the Infiniium 90000 Series oscilloscope provide a fast and easy way to verify and debug your PCI Express designs. The PCI Express electrical test software allows you to automatically execute electrical checklist tests and displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your design passed or failed each test.



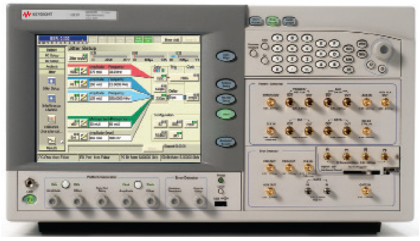
J-BERT M8020A high-performance BERT System

The high-performance Keysight J-BERT M8020A enables fast, accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s. With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements. And, through interactive link training, it can behave like your DUT's link partner. All in all, the J-BERT M8020A will accelerate insight into your design.



J-BERT N4903B high-performance serial BERT

The J-BERT N4903B is a solution for the design and test of digital components, devices and subsystems up to 12.5 Gb/s. It provides complete, calibrated jitter sources for stressed eye testing of receivers. Automated jitter tolerance testing allows quick and accurate compliance and characterization testing. For transmitter analysis, a wide range of error, eye and jitter analysis tools are built-in and provide insight into the underlying causes behind bit errors.



U4301B PCI Express protocol analyzer

Keysight Technologies' high speed U4301B PCI Express 3.0 analyzer module is a protocol analyzer supporting all PCI Express applications from Gen 1 through Gen 3 and speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3) and with link widths from x1 to x16. The U4301B analyzer captures and decodes PCI Express data and displays it in a packet viewer window.

U4305A/B PCIe exerciser & PCIe LTSSM exerciser

The U4305A PCIe 3.0 exerciser with pre-defined LTSSM test cases can help validate the complex and hard-to-test state transitions of a DUT's LTSSM. With the ability to emulate either a root complex or an end point in the same card, the U4305A PCIe 3.0 exerciser can help you validate your device whether it is a server or an add-in card. Powerful validation tools include NVMe emulation with conformance and compliance tests for PCI express and NVMe.

Keysight PCI Express Design and Test Solutions

Keysight PCI Express solutions by technology

		PCI Express technology supported		
Product	**Description**	**1.X**	**2.0**	**3.0**
Physical Layer				
	Infiniium V-Series oscilloscopes	X	X	X
N5393D	PCI Express electrical compliance test application	X	X	X
86100D, 86108B	DCA-X mainframe with precision waveform analyzer module	X	X	X
N4903B	J-BERT high-performance serial BERT, 12.5 Gb/s, 1 channel	X	X	X
M8020A	J-BERT high performance BERT, 16 or 32 Gb/s, 1-4 channels	X	X	X
N4880A	Reference clock multiplier	X	X	X
N4916B	De-emphasis signal converter	X	X	X
N5990A	Automated compliance and device characterization test software	X	X	X
86100D, 54754A	DCA-X mainframe with TDR module	X	X	X
E5071C-TDR	ENA network analyzer with enhanced time domain analysis option	X	X	X
W2212B	ADS Design Software bundle (ADS Core, Transient Convolution, Layout, Momentum G2, EMDS, Ptolemy)	X	X	X
W2352	PCI Express compliance test bench	X	X	X
Data link/transaction Layer				
U4301B	PCIe Gen3 analyzer	X	X	X
U4305A/B	PCIe exerciser	X	X	X
N5323A	PCIe jammer	X	X	

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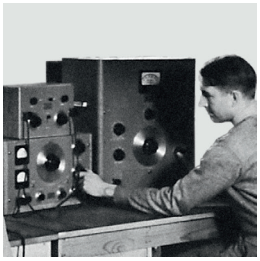

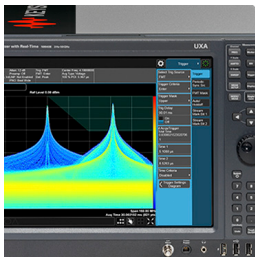

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